AMENDMENTS TO THE CLAIMS

1. (Original) A current mirror, comprising:

a first leg comprising a reference current source operable to generate a reference current;

a first mirror current leg comprising a first P-type CMOS transistor and a first N-type transistor;

a second mirror current leg comprising a second P-Type CMOS transistor and a second N-type transistor;

a load leg comprising a third P-type transistor and a load; and

compensation circuitry operable to compensate for gate current leakage in said first, second and third P-type CMOS transistors.

2. (Original) The current source according to claim 1, wherein said reference current is passed through an N-type CMOS transistor connected in a diode configuration.

3. (Original) The current mirror according to claim 1, wherein said compensation circuitry comprises first and second P-type compensation transistors.

4. (Currently Amended) The current mirror according to claim 3, wherein said first compensation transistor is connected in a diode configuration and is operable to sense and provide ~~the~~ a portion of ~~the~~ a ~~copied~~ reference current that is lost due to gate current leakage of said first, second and third P-type CMOS transistors.

5. (Original) The current mirror according to claim 4, wherein said second P-type compensation transistor generates a compensation current equal to the portion of the copied reference current that is lost due to the gate current leakage of said first, second and third P-type CMOS transistors.

6. (Original) The current mirror according to claim 5, wherein said load comprises a charge pump circuit for a phase-locked loop.

7. (Original) The current mirror according to claim 5, wherein said current mirror comprises at least three output current sources.

8. (Original) The current mirror according claim 7, wherein current mirror comprises a first sensing transistor in a diode configuration and at least three compensation devices to compensate for gate current leakage in said first, second and third P-type CMOS transistors.

9. (Original) The current mirror according to claim 8, wherein said compensation devices comprise P-type CMOS transistors.

10. (Original) The current mirror according to claim 9, wherein said three output current sources each comprise at least one P-type CMOS transistor and wherein said compensation devices compensate for gate current leakage in said P-type CMOS transistors.

11. (Currently Amended) A method of operating a current mirror circuit having a reference leg, first and second mirror legs and a leg load each comprising at least one P-type CMOS transistor ~~and a load leg,~~ comprising:

generating a known reference current in said reference leg of said current mirror circuit;

using said reference current to control the flow of current in said first and second mirror legs and said load leg of said current mirror circuit;

compensating for gate current leakage in said P-type CMOS transistors in said first and second mirror legs and the output load leg, thereby generating a current flow in said load leg equal to the current flow in said reference leg.

12. (Original) The method according to claim 11, wherein said reference current is passed through an N-type CMOS transistor connected in a diode configuration.

13. (Currently Amended) The method according to claim 12, wherein said compensation ~~circuitry~~ comprises first and second P-type compensation transistors.

14. (Currently Amended) The method according to claim 13, wherein said first compensation transistor senses and generates ~~the~~ a compensation current equal to the sum of all ~~net~~ gate current leakage through the diode connection of the first P-type CMOS transistor in the first mirror leg of said all P-type CMOS transistors.

15. (Currently Amended) The method according to claim 14, wherein said second P-type compensation transistor copies the compensation current from the first P-type compensation transistor and adds the compensation current to ~~the~~ a mismatched output current.

16. (Original) The method according to claim 15, wherein said load comprises a charge pump circuit for a phase-locked loop.

17. (Currently Amended) The method according to claim 15, wherein said current mirror comprises at least three output ~~load~~ current source legs.

18. (Original) The method according claim 17, wherein said current mirror comprises at least three compensation devices plus the very first sensing compensation device to compensate for gate current leakage in said all legs containing a P-type CMOS transistor.

19. (Original) The method according to claim 18, wherein said compensation devices comprise P-type CMOS transistor.

20. (Currently Amended) The method according to claim 19, wherein said three output current ~~mirror~~ source legs each comprise at least one P-type CMOS transistor and said three current compensation devices each provide compensation for all of said P-type CMOS transistors.